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A RISC-V 32-bit microprocessor based on two-dimensional semiconductors

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Recently the quest for post-silicon semiconductors has escalated owing to the inherent limitations of conventional bulk semiconductors, which are plagued by issues such as drain-induced barrier lowering, interfacial-scattering-induced mobility degradation and a constrained current on/off ratio determined by semiconductor bandwidth. These challenges have prompted the search for more advanced materials, with atomic-layer-thick two-dimensional (2D) semiconductors emerging as a potential solution. Following over a decade of research advances, recent developments[1–3] in wafer-scale growth and device fabrication have led to breakthroughs in 2D semiconductor electronics. However, the level of integration remains constrained to a few hundred transistors. We describe a reduced instruction set computing architecture (RISC-V) microprocessor capable of executing standard 32-bit instructions on 5,900 MoS_2 transistors and a complete standard cell library based on 2D semiconductor technology. The library contains 25 types of logic units. In alignment with advances in silicon integrated circuits, we also co-optimized the process flow and design of the 2D logic circuits. Our combined manufacturing and design methodology has overcome the significant challenges associated with wafer-scale integration of 2D circuits and enabled a pioneering prototype of an MoS_2 microprocessor that exemplifies the potential of 2D integrated-circuit technology beyond silicon.

After years of research, significant progress has been made in the development of two-dimensional (2D) semiconductors, including wafer-scale growth, band-structure engineering and device optimization[1–3]. In particular, high-performance 12-inch and atomic-layer-thick MoS_2 films have been successfully synthesized[1,4–6], low-resistance van der Waals source-drain contacts have been realized for 2D transistors[2,7–12] and high-quality dielectric formation has also recently been achieved in the 2D channel[3,13–19]. The individual metrics of 2D transistors are already competitive and aligned well with the technical metrics envisioned in IRDS 2022[20], indicative of an excellent beyond-silicon material candidate.

However, to further advance 2D semiconductor electronics, it is imperative that efforts towards very large-scale integration (VLSI) be undertaken by both the academic and industrial communities. Jayachandran et al. recently demonstrated progress by integrating MoS_2 and WSe_2 in a three-dimensional stack[21], which highlights the immense potential for future industry-level integration with silicon integrated circuits. Despite the encouraging progress in array-level demonstrations of high-performance 2D transistors, the development of 2D integrated circuits to an industrial standard is still in its early stages. Importantly, there is still a considerable disparity between functional systems comprising hundreds of transistors (such as a 1-bit adder)[22–26] and those that consist of billions of transistors (such as a high-performance processor). Looking back at the history of the commercialization of silicon integrated circuits, the transition from manufacturing isolated logic gates to the Intel 4004 microprocessor, which has 2,000 silicon transistors, was a major milestone. Similarly, 2D electronics faces three main challenges if it is to achieve a comparable breakthrough:

1. Synergistic optimization of device processing: Given the greater sensitivity of carriers in atomic-thickness 2D channels to their environment than in silicon[26–29], it is important to incorporate innovative process techniques specific to 2D semiconductors while ensuring compatibility with silicon integrated circuits for viable manufacturing.
2. From transistors to circuits: To create functional integrated circuits from uniformly distributed, homogeneous 2D transistors, experience in silicon integrated-circuit manufacturing, including both front-end of line (FEOL) and back-end of line (BEOL), is paramount. A systematic study of material and process co-optimization is also required.
3. New circuit architecture: Silicon integrated-circuit designs are well established, but they may not be adaptable to emerging fields such as edge computing and intelligent sensing, where 2D semiconductors are expected to excel[30–33].

To tackle these challenges, we used a 4-inch MoS_2 wafer to enable a demonstration of a beyond-silicon microprocessor: RV32-WUJI, for which we have achieved: (1) Wafer-level integration based on a

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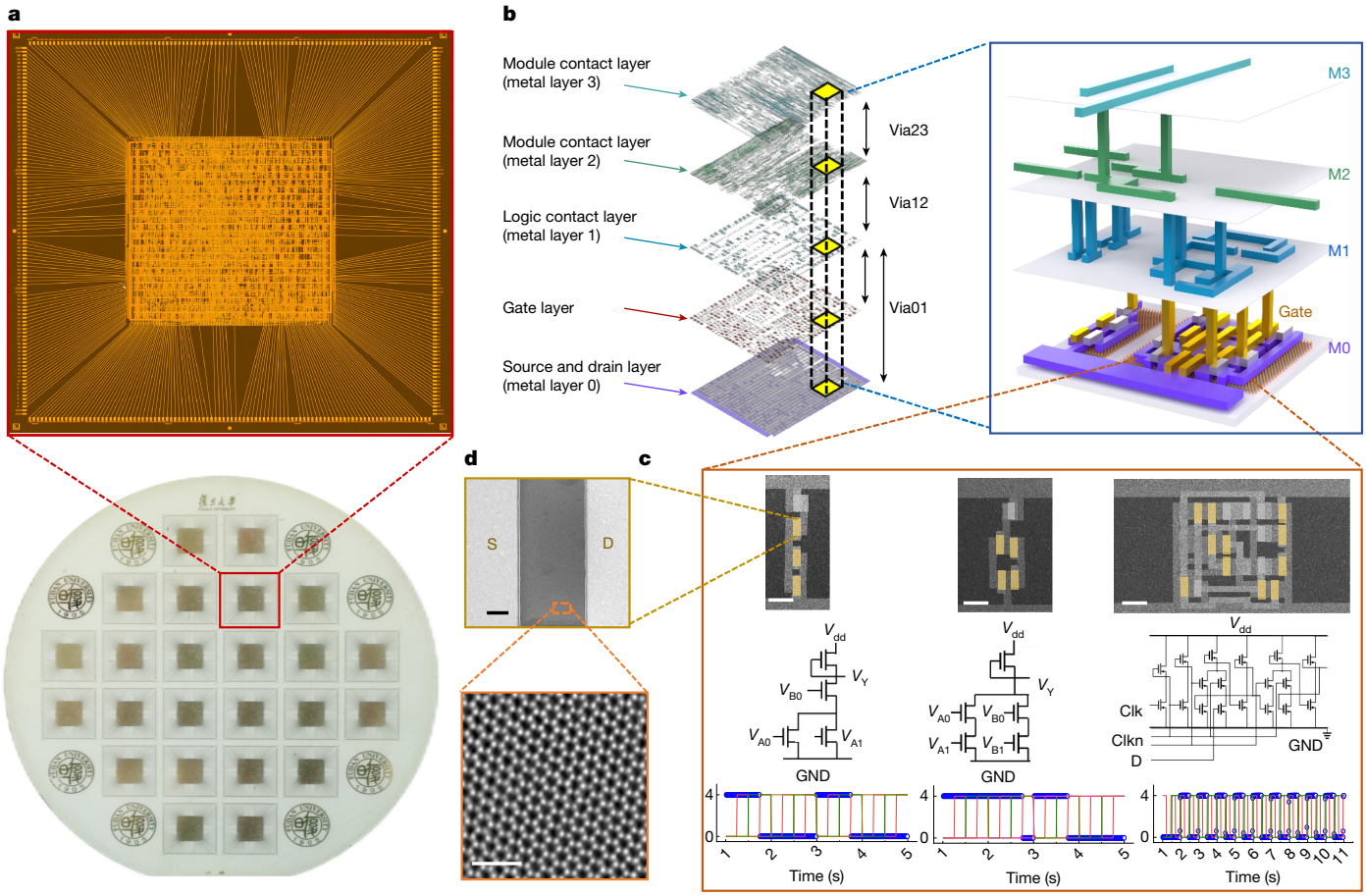


Fig. 1 | RV32-WUJI. a, Bottom, 24 WUJI chips produced on a 4-inch sapphire wafer. Top, zoomed-in optical microscope image showing a single die with an area of 6 mm × 6 mm, consisting of 5,900 MoS_2 transistors, with input and output pads placed around the periphery. **b**, Schematic illustration depicting the physical layout of an RV32-WUJI die, with each layer drawn to scale. The bottom layer consists of MoS_2 synthesized on a sapphire wafer. **c**, SEM images of OAI21, AOI22 and 1-bit register logic gate units (gate electrodes have false colours for the different gate metals) and the corresponding circuit schematics and experimentally measured waveforms. **d**, SEM image of the transistor channel region (top) and a zoomed-in high-resolution transmission electron microscopy image showing the atomic structure of MoS_2 (bottom). Scale bars, 10 μm (**c**), 1 μm (**d**, top) and 1 nm (**d**, bottom). clk, clock; clkn, negative clock; D, drain; GND, ground; S, source; V_{B0}, the voltage of the input port B0; V_{B1}, the voltage of the input port B1; V_{A0}, the voltage of the input port A0; V_{A1}, the voltage of the input port A1; V_Y, the voltage of the output port Y.

top-gate transistor structure and four interconnected layers, which is compatible with mainstream silicon complementary metal–oxide–semiconductor (CMOS) technology. (2) A digital computing functional circuit consisting of over 5,900 MoS_2 transistors capable of performing basic digital operations in the standard RISC-V 32-bit integer (RV32I) instruction set. (3) A complete standard cell library based on 2D semiconductor technology. The library contains 25 types of logic units. The manufacturing yield was 99.77%. (4) A low power consumption of 0.43 mW when the RV32-WUJI is operated at a frequency of 1 kHz.

Fabrication of RV32-WUJI

The RV32-WUJI was fabricated entirely from MoS_2 field-effect transistors (FETs) on a 4-inch substrate and in a VLSI-compatible fashion. The process flow is described in Extended Data Fig. 1b. It features a top-gate FET structure[34], which was developed for effective integration with existing CMOS technologies. Figure 1a has a photograph of the complete wafer (see Supplementary Fig. 1 for wafer-scale material characterization) and an optical microscopic image of an individual RV32-WUJI die. It is one of the largest electronic circuits to date built using 2D semiconductors, comprising 5,900 MoS_2 FETs and a maximum logic path of 17 stages of cascaded logic elements positioned between flip-flops, which necessitate their sequential evaluation within a single clock cycle. The system is powered by a supply voltage (V_{dd}) of 4 V and is regulated by an external clock signal. The circuit is configured to operate independently, without any external biasing or control signals.

The RV32-WUJI has a four-layer structure, as shown in Fig. 1b. The source and drain layer (M0) and the gate layer, which contain the underlying operating transistors, are formed during the FEOL process. The BEOL process forms the logic connect layer (M1) and the module connect layers (M2 and M3). The logic connect layer (M1) connects the transistors to form basic logic units. The module connect layers (M2 and M3) bridge the basic logic units to form a fully functional chip. Figure 1c shows scanning electron microscope (SEM) images of three typical logic modules (OAI21, AOI22 and a register). The corresponding circuit structures and operation logic are presented in the lower panel. Figure 1d displays a magnified SEM image of the bare MoS_2 channel before the deposition of the top-gate stack and also an atomic-resolution image of the fine lattice arrangement by transmission electron microscopy.

In RV32-WUJI, the underlying MoS_2 FETs are built on an insulating sapphire substrate, which completely isolates them electronically from each other. This is like silicon-on-insulator technology, which reduces the capacitance and current leakage across the transistors. Additionally, the MoS_2 channel is only three atoms thick and is free of dangling bonds in the plane, making it more favourable for electrostatic control in a planar transistor structure. To achieve a complex MoS_2 VLSI,

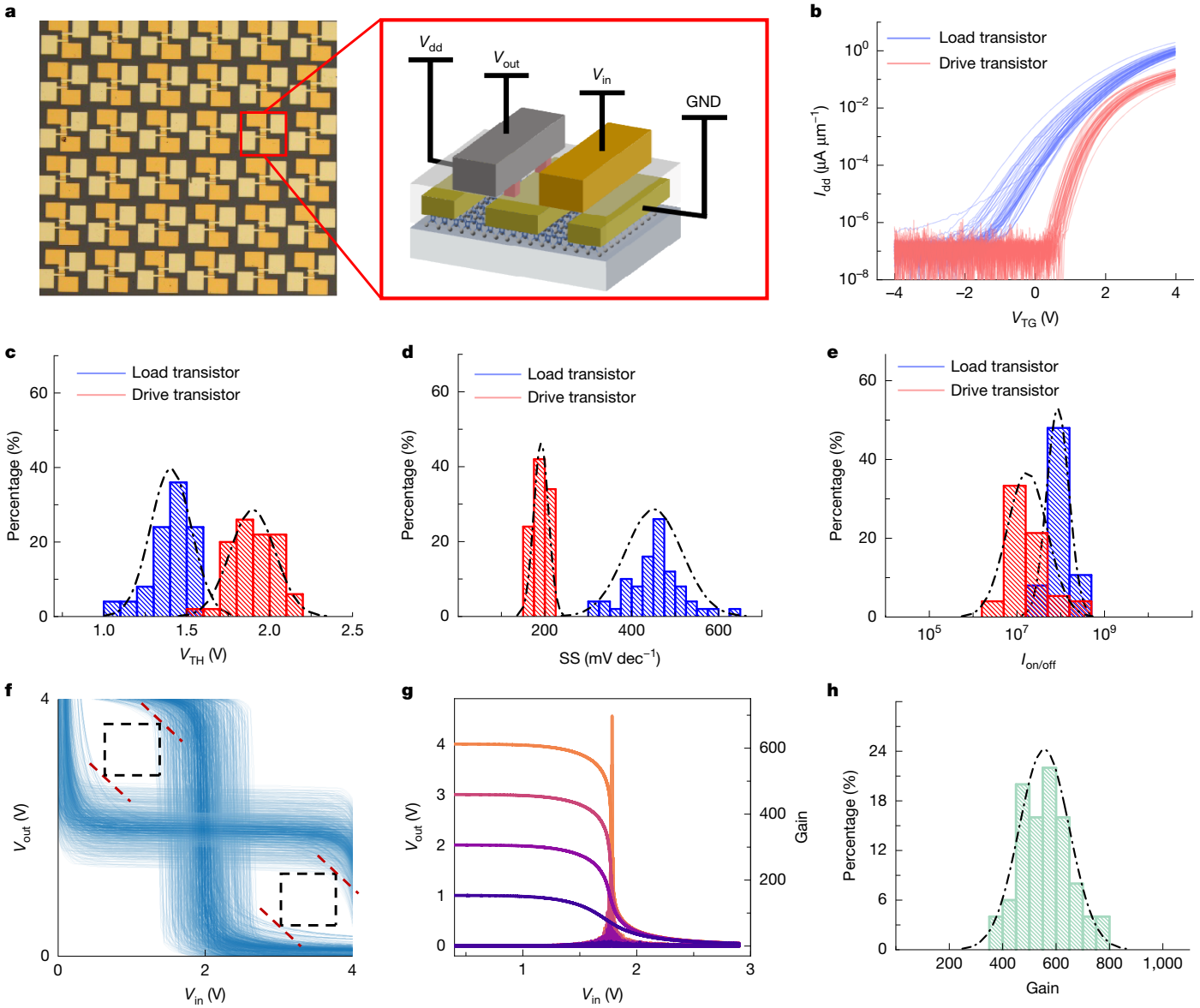
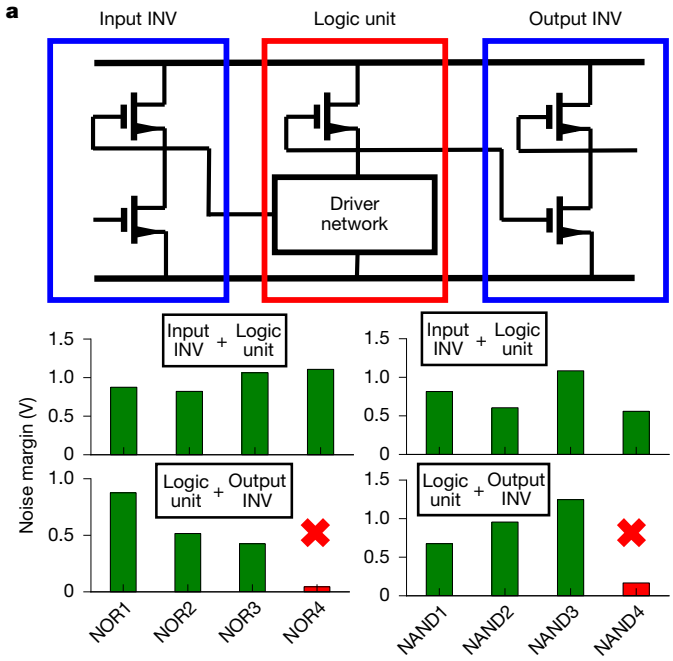


Fig. 2 | FET and inverter. a, Transistor schematics with different gate metals. **b**, Transfer characteristic curves of the load and drive transistors that make up the inverter; the number of load transistors and drive transistors each amount to 50. **c**–**e**, Statistical distributions of V_{TH} (**c**), the subthreshold swing (**d**) and the on/off ratio (I_{on}/I_{off}) (**e**) for 50 transistors. **f**, Static voltage transfer characteristics with noise tolerance of 900 inverters. **g**, Gains calculated from the transfer curves of a typical inverter at different voltages. **h**, Statistical distribution of the gain values, demonstrating the gain of 50 inverters. SS, subthreshold swing; V_{TG}, the voltage of top gate.

it is essential to develop effective process strategies for the key steps, such as forming the ohmic contacts[2,7–12], depositing high-quality gate dielectrics[3,13–19] and implementing an effective doping strategy[35–37]. It is also important to note that these key process steps in integration are strongly coupled with each other, as the atomic-layer-thick channel is extremely sensitive to any process treatment.

Previous studies have confirmed that wafer-level processing of discrete FET arrays can achieve a high yield[26]. However, forming a VLSI that integrates several functional units into a single chip is much more complex. For instance, accurately controlling the threshold voltage (V_{TH}) of the load and driver transistors is necessary for the reference switching threshold voltage (V_M) of an inverter circuit, which is a basic logic unit. Our RV32-WUJI is based on the MoS_2 n-type metal–oxide–semiconductor architecture. Precise control of V_{TH} at wafer scale is crucial for achieving a high overall yield. In conventional semiconductor technologies, V_{TH} is commonly controlled by ion implantation, but this method is unsuitable here because it causes severe lattice damage to the fragile 2D crystal structure. Thus, V_{TH} is modulated in our RV32-WUJI through two methods: (1) by applying aluminium (Al) or gold (Au) metal gates with different work functions to enable either the accumulation or depletion state of MoS_2 channels (see Fig. 2b and Methods for more details) and (2) through seeding-layer optimization for high-k dielectric-layer deposition on top of the MoS_2 channel. Such combined strategies can efficiently tune the V_{TH} of MoS_2 FETs for circuit-level matching and optimization in M1 and the gate layer.

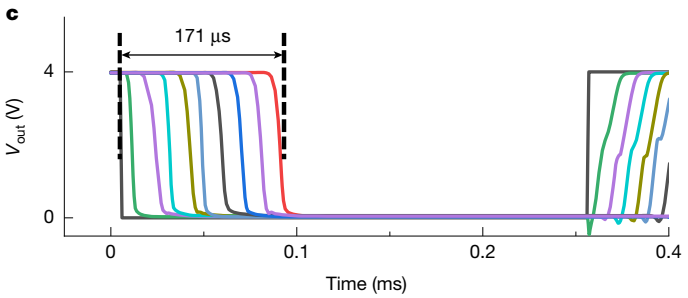
These wafer-scale fabrication procedures, coupled with the intricate nature of the 2D semiconductors, inevitably results in a multitude of impacts on device performance, thus posing significant challenges for optimizing the complete process flow. To address these challenges and ensure sufficient overall yield for 2D VLSI, we adopted a systematic co-optimization strategy integrated with a machine learning methodology[26], which enabled us to decompose and independently analyse the



b

Noise margin of logic unit (V)

NOR	NOR1	NOR2	NOR3	NOR4
	0.875	0.515	0.425	0.045
NAND	NAND1	NAND2	NAND3	NAND4
	0.675	0.605	1.083	0.166
AOI	AOI21	AOI22	AOI31	AOI32
	0.584	0.754	0.485	0.435
	AOI33	AOI211	AOI221	AOI222
	0.184	0.613	0.487	0.057
OAI	OAI21	OAI22	OAI31	OAI32
	0.624	0.542	0.412	0.457
	OAI33	OAI211	OAI221	OAI222
	0.117	0.403	0.094	0.054



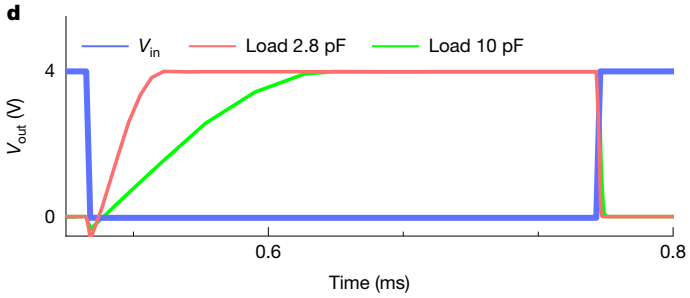


Fig. 3 | Logic cell. a, Noise tolerance of a logic unit that is driven by an inverter and drives another inverter. The panels below display, respectively, the noise margins of NOR and NAND series logic units when driven by an inverter and when driving an inverter. **b**, The noise margins of common single-stage load logic circuits. Logic units with noise margins of less than 5% of V_{dd} are coloured red. **c**, The longest logic gate path, which has 17 stages, has a maximum delay of 171 µs. **d**, The time-resolved performance of an inverter is dictated by its ability to handle various loads while maintaining its intended functionality. AOI, AND-OR-invert; INV, inverter; OAI, OR-AND-invert.

specific contribution of each process step to device performance metrics (Extended Data Fig. 1a), thereby improving the yield of wafer-level 2D integrated-circuit manufacturing. To assess the efficacy of the methodology, three batches of MoS_2 wafers were prepared, each containing 7,000 transistors, of these, 800 transistors were randomly selected for testing. The acquired V_{TH}, subthreshold swing and I_{on}/I_{off} distributions are illustrated in Supplementary Fig. 2. The overall transistor yield reached 99.92%, thereby establishing the feasibility of large-scale digital integrated-circuit manufacture.

For the BEOL process for M1–M3, the oxide isolation layer, known as the interlayer dielectric, can also affect V_{TH} and V_M. For this reason, we also carefully optimized the deposition of the interlayer dielectric. The shift of the inverter V_M did not exceed 4.4% of V_{dd} after the interlayer dielectric had formed (see Extended Data Fig. 2 for details). After all back-end connections had been completed, the inverter V_M shift did not exceed 6.2% of V_{dd}. Such stability in the back-end process is highly desirable for VLSI of 2D semiconductors.

Transistor-level matching

The basic logic unit of the WUJI architecture is an enhancement-and-depletion mode inverter (Fig. 2a), which is suitable for n-type MoS_2 transistors. As mentioned above, the load transistor of the inverter uses Al metal as its top-gate electrode, whereas the driver transistor uses Au. Figure 2b shows the transfer curves of 50 MoS_2 transistors with an Au top gate and another batch of 50 transistors with Al top gates. The threshold voltage (V_{TH}) shows a significant difference, which is primarily due to the different work functions of Au and Al (see Supplementary Fig. 4 for details). The distinct V_{TH} enables the enhancement-and-depletion mode inverter to operate effectively, with gains as high as 760 for a working voltage of 4 V at room temperature and ambient conditions (Fig. 2h).

The uniformity of the inverters is a key factor when fabricating integrated circuits. A 30 × 30 array of 900 inverters was fabricated to determine the inverter yields in the 6-mm × 6-mm region of the WUJI chip. The transfer characteristic curves of all the inverters are shown in Fig. 2f. We found that 898 out of 900 inverters worked correctly with a yield of 99.77% and an overall noise tolerance of 0.5 V. The switching voltages of the working inverters were distributed in the range 1.4 to 2.5 V (Supplementary Fig. 4), and the average gain of all 898 inverters exceeded 550. These uniform and high-performance inverters provide the device foundation for implementing advanced digital logic circuits.

Logic units in RV32-WUJI

Inverters are the basis of all logic units. Based on the above inverter characteristics, we built a 2D process design kit with a complete basic

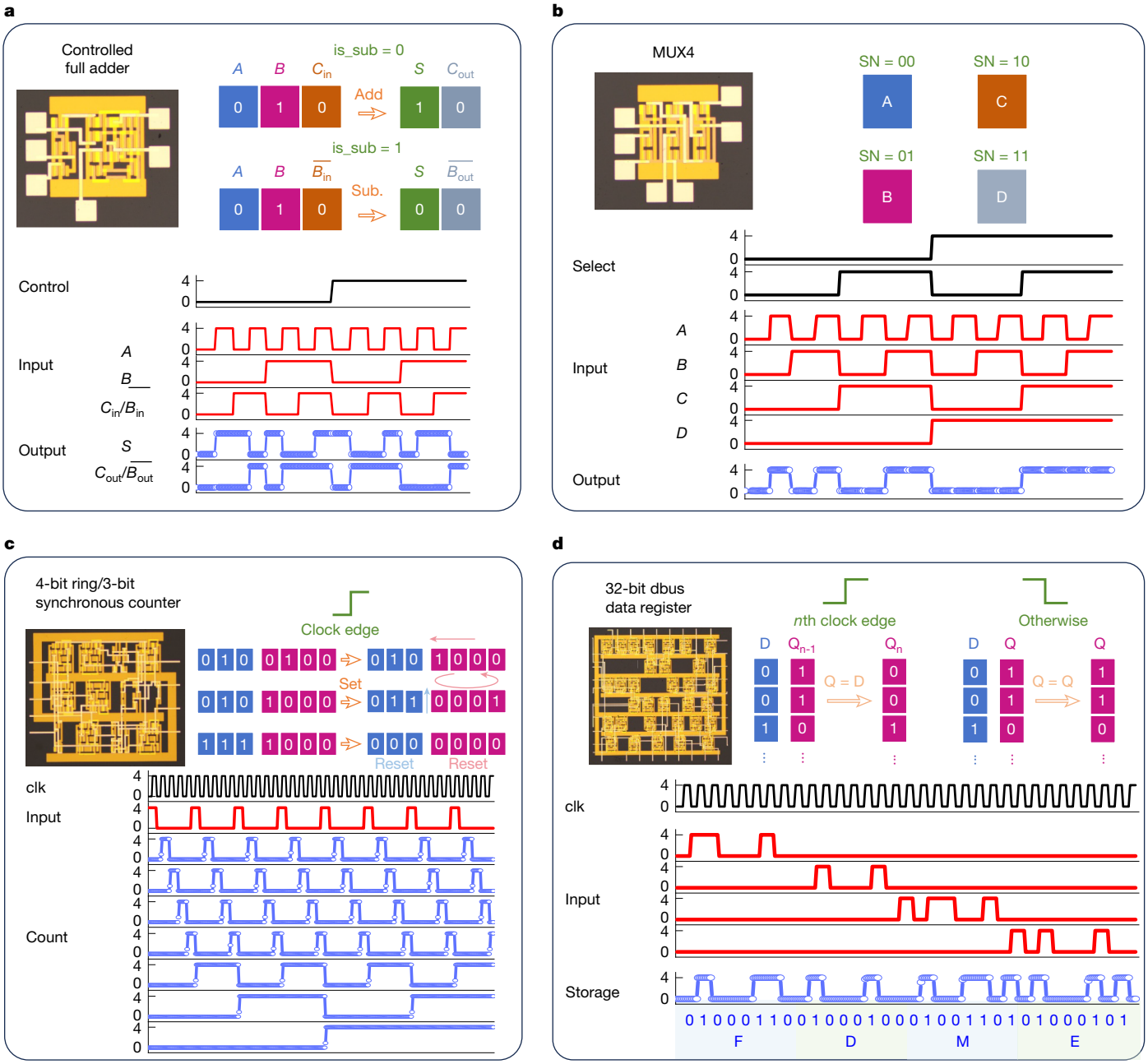


Fig. 4 | Core unit. a–**d**, Circuit structure (upper left), basic logic function (upper right) and typical experimentally measured logic output (lower graph) of a controlled full adder (**a**), 4-input multiplexer (**b**), 4-bit loop counter and 3-bit synchronous serial counter (**c**), and 32-bit register (**d**). The bottom of **d** is an experimental demonstration of the storage of four 8-bit ASCII codes for 'F', 'D', 'M' and 'E' (for more details, see Extended Data Fig. 5e). MUX, multiplexer; Sub., subtract. SN, the n-bit select signal.

logic-unit library. Unlike conventional CMOS logic units, which can use both load and driver transistor networks, logic units constructed with n-type MoS_2 transistors can use only the driver transistor network, and only one transistor can be used for the load portion. This inevitably leads to load-matching problems in MoS_2 logic circuit design. To address this issue, we tested and calculated the noise margins for the input and output loads of the logic units. As shown in Fig. 3a, an inverter was added to both the input and output terminals of the logic unit, and its noise margin was tested by modifying the drive network (Extended Data Fig. 3a,b). After that, we summarized the input–output margin maps for various single-stage logic gates and conducted a detailed analysis of the specific impact of different combinations of logic units on these margin maps. We also compiled the minimum margin values for 25 combinations of single-stage logic gates (Extended Data Fig. 3c) operating at 4 V. Of these, 18 logic gates were selected as practical modelling units in the process design kit for application, as shown in Fig. 3b.

We then conducted a comprehensive examination of the delay in the longest path of RV32-WUJI, which revealed a maximum delay of 171 µs (Fig. 3c). This indicates that WUJI is capable of supporting a maximum operating frequency of up to a few kilohertz. The load versus drive correlation is illustrated in Fig. 3d, which confirmed that the design allows a single logic unit to drive a maximum of four loads (10 pF loads), thereby satisfying the requisite number of logic-unit load combinations. To investigate the variability of the core speed, different supply voltages were applied to the longest delay path (Supplementary Fig. 6). The circuit delay gradually increased with the supply voltage, primarily

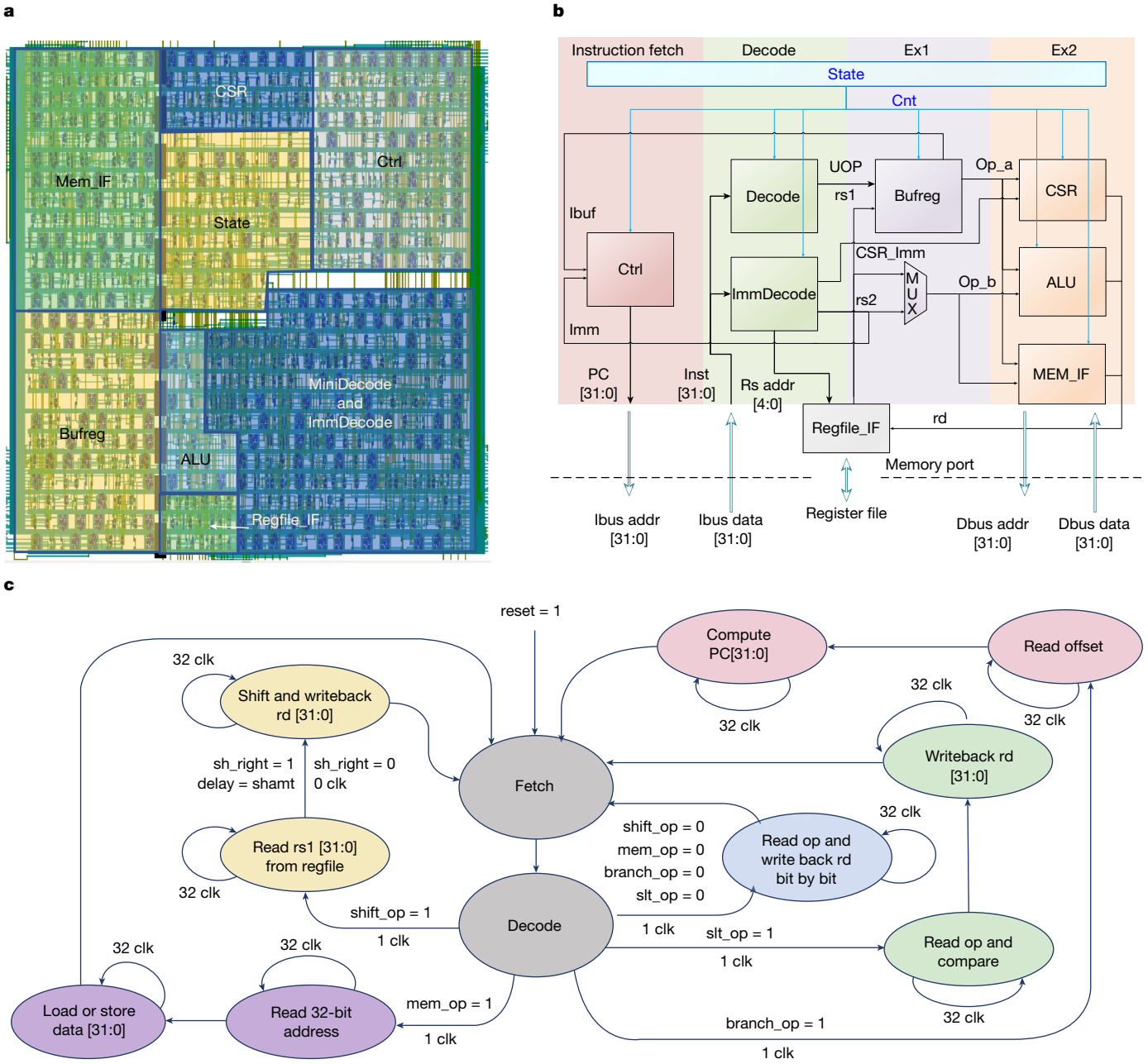


Fig. 5 | Architecture and design of RV32-WUJI. a, Architecture of a RV32-WUJI core consisting of nine basic modules. **b**, Schematic data path through the nine modules. **c**, Schematic state machine depicting the instruction flow in WUJI. addr, address; ALU, arithmetic logic unit; branch_op, branch operation; Bufreg, buffer register; Cnt, counter; CSR, control status register; Ctrl, control module; Ibuf, instruction buffer; ibus or Ibus, instruction bus; Imm, immediate value; ImmDecode, immediate-number-decoding module; Inst, instruction; MEM_IF, memory interface; mem_op, memory operation; MiniDecode, instruction-decoding module; op_a, operand a; op_b, operand b; PC, program counter; rd, destination register; Regfile_IF, register file interface; shamt, shift amount; shift_op; shift operation; sh_right, shift right; slt_op, set-on-less-than operation; UOP, micro-operation.

because our load transistors operate in the subthreshold region where the output current does not increase significantly with increasing load. As the operating voltage was increased, the resulting greater capacitor charging led to a longer maximum circuit delay.

We next explored the yield distribution of the logic circuits. We considered multi-bit shift registers owing to the convenience of circuit design and measurement. The yield rates of multi-bit registers with various numbers of transistors are illustrated in Supplementary Fig. 7. The yield of 8-bit registers, each with 144 transistors, reached 71% at the wafer scale. As the size of the circuit was increased, the yield began to decrease, reaching approximately 7% for a 64-bit register with 1,152 transistors. This can reasonably be attributed to factors such as the relatively low grade of the clean room in our laboratory (compared to an industrial-grade cleanroom) and the stability of the processing tools used. It is, therefore, necessary to further optimize and improve the manufacturing process of VLSI 2D integrated circuits in a more industrial manner.

Core modules in the RV32-WUJI

Because we used the optimized standard unit library described above, we could use electronic design automation tools to design and

construct each module of the RV32-WUJI, which will ultimately form a complete functional microprocessor. The functions and implementations of each module are slightly different and can be summarized into four key functions: data operation, data selection, state counting and data storage. Figure 4 displays the four typical circuits that correspond to these functions: controlled full adder, multiplexer, counter and 32-bit register (see Extended Data Fig. 5a–d for their circuit schematics). Each subgraph shows the corresponding circuit structure, a functional schematic and the experimentally measured output waveform.

Architecture of the RV32-WUJI

The aforementioned modules were used to create our RV32-WUJI chip, which is based on the RV32I instruction set. The RV32-WUJI has a 1-bit arithmetic logic unit for performing operations, a control status register module, an instruction-decoding module, an immediate-number-decoding module and a control module where the program counter is situated. The chip also has a buffer register module, which stores intermediate results, a small state machine that monitors the execution status of instructions and interface modules for the register file and the memory, as depicted in Fig. 5a. These modules include the core components depicted in Fig. 4, along with supplementary components depicted in Extended Data Fig. 6.

The complete data path in WUJI is shown in Fig. 5b. In the first clock cycle of a new instruction, the control module sends the 32-bit program counter with the enable signal pc_valid to the instruction bus. This is followed by the reception and decoding of the instruction in subsequent cycles. The data are processed by the arithmetic logic unit. The first operand Op_a is obtained from the register file, and the second operand Op_b is selected through a multiplexer at 1 bit per clock cycle. The arithmetic operation between Op_a and Op_b is ultimately completed after 32 clock cycles. Our complete instruction set for the RV32-WUJI can be found in Extended Data Table 1. To implement these instructions, we adopted a serial-processing architecture, which is described by the state machine in Fig. 5c (Methods). The architecture of this arithmetic logic unit with a 32-bit serial data path was designed to reduce static power consumption and hardware overhead to address power efficiency and cost concerns rather than performance requirements, thereby making it suitable for use in scenarios such as edge-embedded environments for small internet of things devices.

We used a functional RV32-WUJI chip to implement a complete arithmetic operation (Extended Data Fig. 7). The figure shows executive waveforms for the addition calculations '1946 + 25 = 1971' and '1971 + 53 = 2024'. Here, 1946 and 1971 represent the years in which ENIAC (the first general-purpose programmable electronic digital computer) and the Intel 4004 (the first commercially produced silicon microprocessor) were created. The power consumption for executing these arithmetic operations at 1 kHz is 0.43 mW.

Outlook

This work represents an important milestone in demonstrating that the integration of 2D semiconductors into large-scale functional circuits is now feasible. Our laboratory-level fabrication capability enabled us to fabricate a RISC-V microprocessor consisting of 5,900 MoS_2 transistors, which is one of the most complex functional circuits based on 2D semiconductors to date (Extended Data Table 3). Also note that the entire RV32-WUJI chip uses only n-type MoS_2 transistors with a long channel length. This may result in certain limitations in terms of dynamic and power consumption compared to CMOS technology. A more suitable circuit architecture, such as pass-transistor logic, may be a compromise solution for circuits using single-polarity transistors. In the long run, we anticipate that further optimization and innovation in processing and materials will facilitate the realization of 2D CMOS in the short-channel regime. By then, the full potential of 2D semiconductors will be unlocked.

Online content

Any methods, additional references, Nature Portfolio reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41586-025-08759-9.

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Methods

Wafer-scale MoS_2 film growth

The 4-inch MoS_2 film on a sapphire substrate underwent O_2 plasma treatment to ensure cleanliness and optimal uniformity for film growth (see Supplementary Information for detailed material characterization). To improve the uniformity of the MoS_2 film obtained, a high-quality amorphous Al_2O_3 thin film with a thickness of 20 nm was deposited as a growth promotion layer using thermal atomic layer deposition (MNT-S300Oz-L4). A sponge-like mixer made of MoO_3/graphene oxide with dimensions of $12 \times 12 \times 1\ mm^3$ was placed directly below the inverted growth substrate in a quartz tube furnace with a diameter of 200 mm. Pure sulfur sources were positioned symmetrically at both ends of the quartz tube. The growth chamber was evacuated to a pressure below 1 Pa and then purged with argon gas to ensure a contamination-free environment. The MoO_3/graphene oxide sponge and sulfur precursors were heated to 700 °C and 220 °C, respectively, under a consistent internal chamber vacuum of 0.02 Pa. The growth process lasted for 15 min in the static growth phase. Most of the 4-inch MoS_2 wafers were supplied by Shenzhen Six Carbon Technology Inc.

Transistor fabrication

During the FEOL processing of the RV32-WUJI, MoS_2 top-gated transistors were fabricated directly onto the as-synthesized MoS_2 film without the need for an extra transfer process. Features were patterned by photolithography using a maskless laser direct writing system with a wavelength of 405 nm (Durham Microwriter ML-3). The source and drain patterns were defined first, followed by O_2 plasma treatment and the metallization of 35-nm-thick gold by electron-beam evaporation. We then lithographically patterned and protected the active region (the channel region of the MoS_2 transistors) with a photoresist. This was followed by etching all the MoS_2 outside these protected regions using reactive-ion etching in an O_2/Ar mixed atmosphere at 150 W power for 30 s. Next, we fabricated a dual-stack top-gate dielectric consisting of a 1-nm amorphous SiO_2 layer as a seeding layer (and also as a passivation layer to maintain the enhancement-type channel), followed by a 16-nm high-*k* HfO_x layer grown by atomic layer deposition. Two types of metals with different work functions were adopted for the top-gate construction. A 35-nm-thick layer of Au metal was used for the drive transistors, and an Al/Au dual-stack metal (10 nm Al and 25 nm Au) was used for the load transistors. This strategy optimizes the inverter circuit by matching the electrical properties of the load and driver transistors in a stable manner, rather than using other doping strategies. Extended Data Fig. 1b is a schematic of the process flow.

BEOL process and packaging

After we had fabricated the MoS_2 transistor, conventional BEOL metallization was used to define further metal layers (M1–M3) to interconnect the bottom transistors for signal routing and power distribution. To achieve this, vias were etched through the dielectric layer using inductively coupled plasma etching with SF_6 gas at a pressure of 0.8 Pa. The vias were then filled with a stack of Ti/Au/Ti. To create an insulating layer, magnetron sputtering was used to deposit amorphous SiO_x under an Ar atmosphere. For the interlayer interconnections, electron-beam evaporation was used to deposit 40 nm of Au. At the end of BEOL, the wafer underwent a final anneal at 220 °C. More metal was deposited over the input and output pads to thicken them for wire bonding and packaging. The finished wafer was diced into chips, and each RV32-WUJI chip was packaged for testing.

Basic electrical testing

The electrical performance of the transistors and simple logic elements was assessed using a semiconductor device analyser (B1500A, Keysight), which was complemented by a temperature variable probe station. The voltage range used to obtain the characteristic performance curves of the transistors spanned from −4 to 4 V, a range that is compatible with the operational voltage of our logic components. Both the inverters and the other logic elements were designed to operate at 4 V, which we identified as the optimal working voltage to maximize the noise tolerance of our inverters. The gain values of the inverters were meticulously measured across various operating voltages with a fine sampling resolution of 500 μV. This sampling granularity ensured that the readings were free from noise interference, thereby guaranteeing data integrity. Our evaluation of the static power dissipation of the logic elements adhered to a quasi-static test protocol, where an interval of 10 ms was allotted per sample point. The maintenance duration for each logical state spanned 25 sample points, amounting to a total of 250 ms. Such a quasi-static test at a relatively low frequency can effectively eliminate the influence of dynamic power consumption to enable a fair comparison. The distribution of high and low static power consumption for each logic cell was calculated based on its truth table. Subsequently, the average static power consumption was determined by an accumulation of both high and low states. We conducted capacitance testing using an impedance analyser (E4990A, Keysight) to complete the load capacitance testing of the device.

Testing the RV32-WUJI

When the number of inputs to the logical circuit exceeds 6, our semiconductor analyser was no longer able to meet the test requirements. To accommodate the necessary test conditions, a custom-designed probe card was made with 400 pins uniformly distributed along the four sides of the diced chip, thus enabling the simultaneous writing and reading of 400 signals through the I/O ports. A comprehensive datasheet for the RV32-WUJI is presented in Extended Data Table 2.

Layout design

Our process design kit for 2D semiconductors has a comprehensive suite of files including library exchange format (LEF) files, circuit description language (CDL) files, graphical data system (GDS) files and technology files (TFs) for use with ICC2 and Virtuoso, as well as scripts for file conversion and layout routing. The LEF files facilitate an abstract representation of the standard cell library, which is critical for automated placement and routing tools. CDL files are netlist files that describe circuit terminals and connections. All components are described using subcircuits. GDS files are the industry-standard binary format for describing the geometry of masks used in photolithography and include layer and geometric shape information.

VLSI design

The digital front-end design of the RV32-WUJI processor uses the open-source Serv RISC-V CPU[38–42]. The designs of other components adhere to the widely accepted commercial VLSI design workflow. To meet the requirements for processor-scale integrated-circuit development, we first created a standard cell library for verification. With this foundation, we could use a design process and electronic design automation tools that are fully compatible with industrial silicon circuits. This approach allows for the design of integrated circuits using 2D semiconductors of any scale.

RISC-V implementation

The RISC-V implementation is written in Chisel, a high-level hardware description language that allows for high configurability. It was first transformed into the internal language Firrtl and then compiled into the standard register-transfer-level hardware description language, Verilog. The implementation can be easily configured to accommodate various memory capacities and data-path widths to meet different application requirements. Additionally, a test tool known as the Chisel tester allows the use of high-level language libraries to generate test patterns for separate module tests to provide basic functional verification. Through compilation using standard RV32I tool chains, programs such

as hello, coremark and dhrystone were transformed into program codes and initialized into the storage system of our RISC-V implementation. The overall system was then verified to ensure the proper functionality of the register-transfer-level design using Verilator. All simulation waveforms were recorded as value change dump (VCD) files to provide the desired testing patterns.

The next step in developing the RV32-WUJI processor is its physical design, which mainly involves placement and routing and layout versus schematics (LVS) verification. This process relies on the standard cell library, which includes the complete GDS layout files for all logic gates, as well as LEF, TF, LVS and CDL files, among others. The LEF files contain information about the signal-pin positions for the logic gates, whereas the TF files include metal interconnect layer information. The LVS files contain device extraction rules as well as LVS verification settings. The CDL files are netlist files for the logic gates and are like the SPICE format. Using the LEF and TF files, we performed an automatic layout and routing for the input gate-level netlists in Verilog format within Synopsys ICC2 and conducted a preliminary LVS verification. After exporting the GDS layout files for RV32-WUJI, we employed Calibre LVS to extract the SPICE netlists corresponding to the layout using the LVS files, which were then validated against the designed SPICE netlists.

Data path in RV32-WUJI

During the first clock cycle of a new instruction, the control module sends the instruction to the instruction bus of the 32-bit WUJI with the enable signal pc_valid. In the following clock cycle, WUJI receives the 32-bit instruction with the acknowledge signal inst_valid and stores it in the instruction-decoding and immediate-number-decoding modules module, where the instruction is decoded separately into control signals and immediate numbers. The counter in the state module is then initialized and begins counting from 0 to 31 while the data are processed at 1 bit per clock cycle in the arithmetic logic unit. Most instructions involve operations with two pieces of data: Op_a and Op_b. Op_a is obtained from the register file through the register file interface, whereas Op_b is selected by a multiplexer from either the register file or is the immediate number. After 32 clock cycles have been counted by the state module, the 32-bit arithmetic operation between Op_a and Op_b is completed. In certain operations, such as a shift instruction, a 32-bit data value from the register file is stored in the buffer register in the first 32 clock cycles, which is called a stage, and then the data are shifted and written back to the register file in the second stage.

State machine of RV32-WUJI

The state machine shows how instructions execute in a serial-data-path CPU. Simple arithmetic and logical instructions like ADD and ADDI use operands from the register file and immediate values, with results written back to the register file. These one-stage instructions perform calculations and writebacks within 32 clock cycles. In each clock cycle, 1 bit of data, starting from the low bit, is calculated and written back. However, the shift, mem, branch and slt instructions require several stages. Shift instructions need an initial stage to read the data and the shift amount from the register file, and a second stage to write back the shifted data. Left shifts start outputting zero-padded lower bits immediately, whereas right shifts delay sending an output until the shift is complete and so have a shift-amount cycle delay. Memory access instructions first read and calculate the 32-bit address and then write back the 32-bit data in a subsequent stage. Branch instructions first judge the condition and read the offset, then compute the new 32-bit program counter in the next stage. Set-on-less-than instructions compare operands and output 0 or 1. As the result is in the lower bits, the comparison is done in the first stage, with the result written back in the second stage.

Data availability

All data from this study are included in the paper and are available from the corresponding authors upon request. Source data are provided with this paper.

Code availability

All codes used in this study are included in the paper and are available from the corresponding authors upon request.

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Author contributions P.Z. and W.B. proposed this work. W.B. and M.A. directed the fabrication aspects of this project. W.B., S.G., X.D., Y.Z., Q.S., Z.Z., Y.H., J.Z. and C.S. contributed to the development of the FEOL fabrication process. M.A. and Q.Z. contributed to the development of the BEOL fabrication process. S.C. led the short-channel device fabrication. X.Z. performed VLSI design aspects of this project including the creation of the MoS_2 FET process design kit and all standard cells in the MoS_2 FET library. X.Z. also performed the RV32-WUJI physical design and led experimental calibration and testing. J.H. and X.K. led the architectural definition of RV32I-WUJI, including Firrtl, the Verilog hardware description language and the instruction set architecture, and they also wrote the test programs. K.W. contributed to project management. S.W. and J.W. contributed to manuscript preparation. W.B. and P.Z. were in charge, advised and led on all aspects of the project.

Competing interests The authors declare no competing interests.

Additional information
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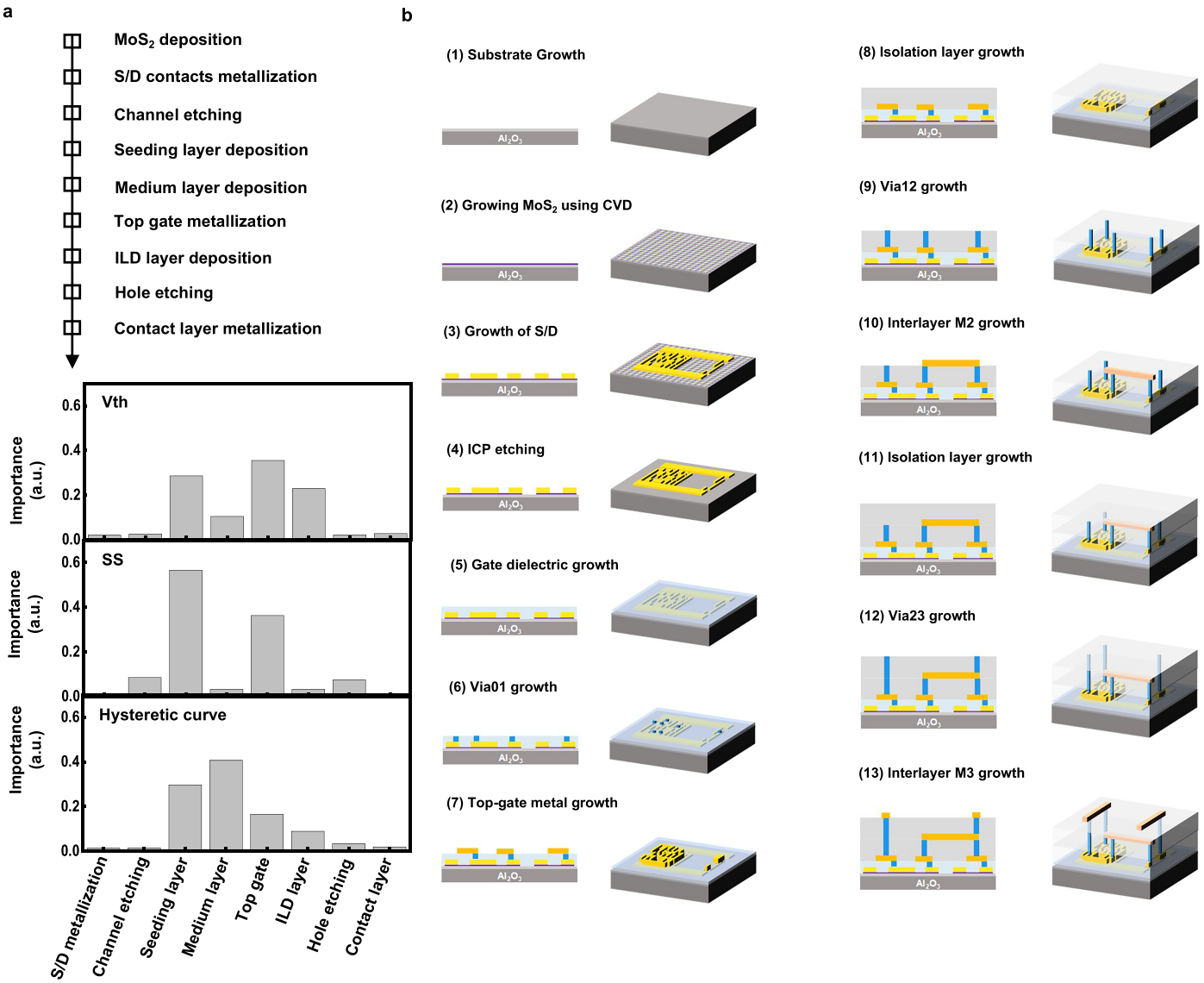
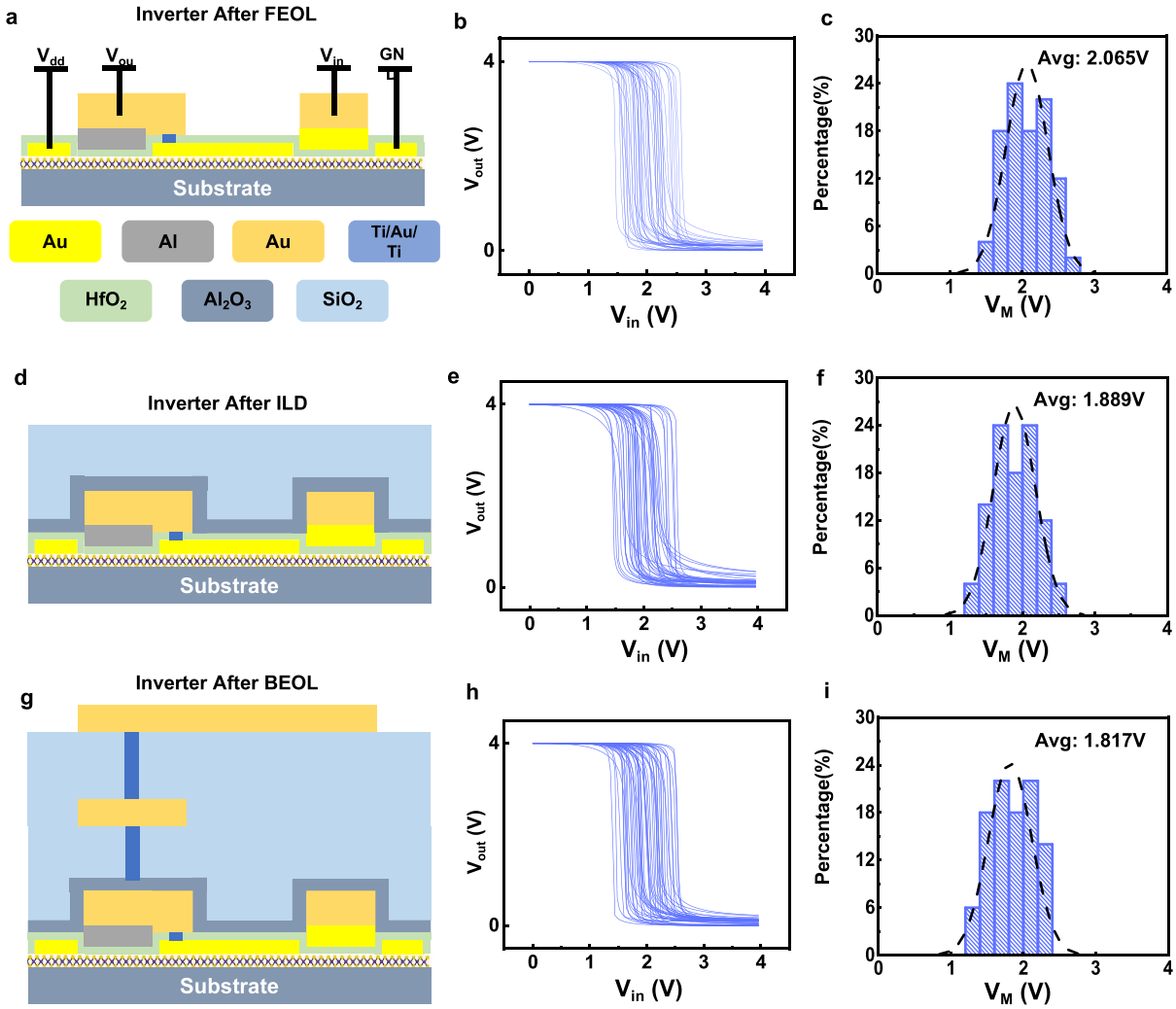
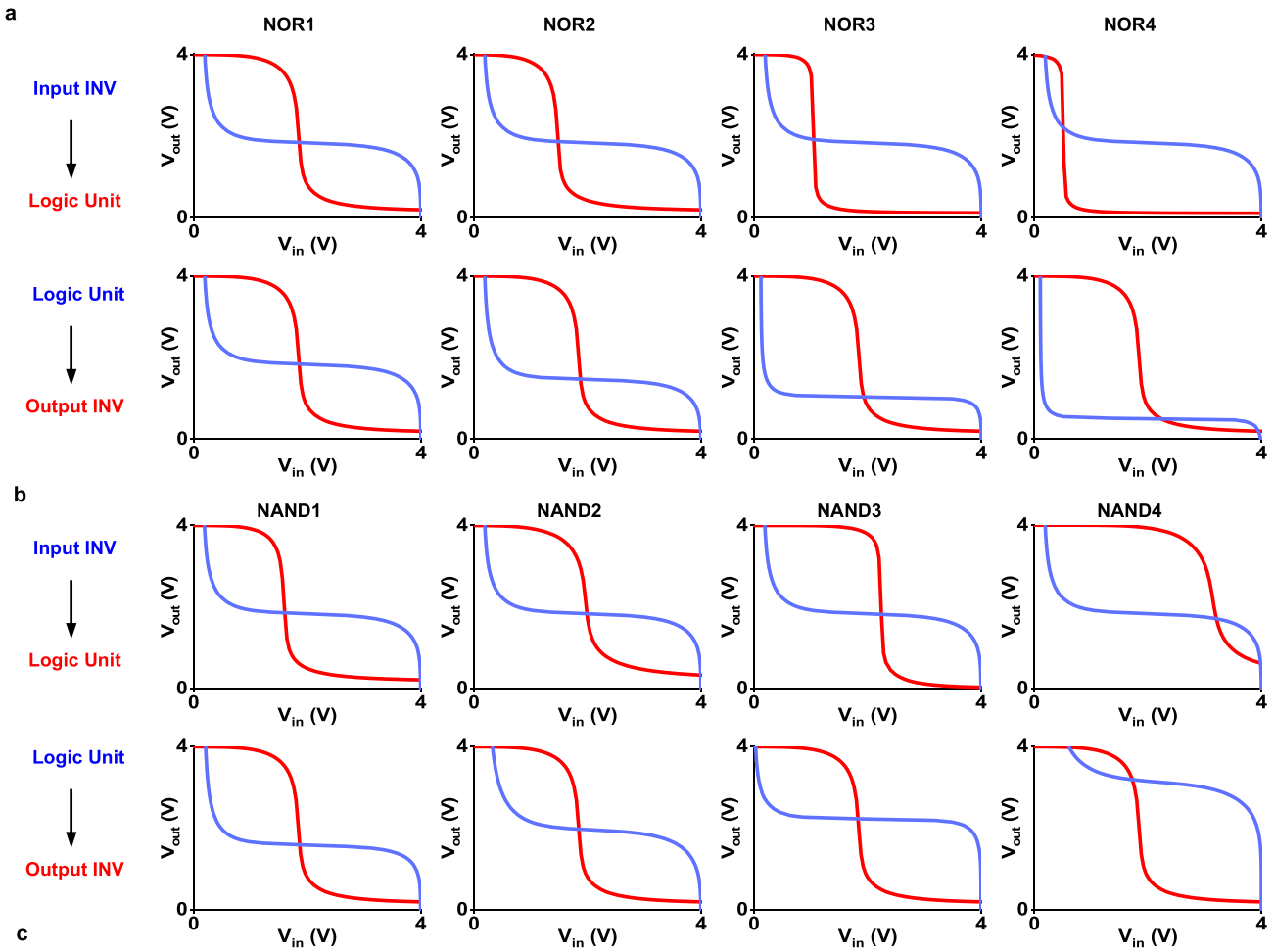


Extended Data Fig. 1 | The impact of process steps on transistor performance and the complete fabrication process flow for RV32-WUJI. a, We divided the process steps for wafer-level circuits into nine main modules and utilized machine learning to analyze the transistor performance under thousands of different process conditions, thereby studying in detail the impact of each process step on transistor performance. This approach effectively helped us determine the optimal wafer-level process flow. **b**, The integration at the wafer level involves four metal layers (M0-M3) and can be divided into three main parts: **(1-2)**, synthesis of MoS_2 on a rigid substrate; **(3-7)**, preparation of the MoS_2 transistors; and **(8-13)**, back-end-of-line process. The diagram illustrates the interconnection of a full adder with an inverter.



Extended Data Fig. 2 | The stability control of the logic circuits in the back-end of line integration. An example is provided using the voltage transfer characteristic of the inverter unit. After completion of the front-end of line process **(a-c)**, the average switching voltage (V_M) of the inverter is 2.065 V. After the subsequent deposition of the inter-layer dielectric (ILD) isolation layer **(d-f)**, V_M experiences a slight negative shift and becomes 1.889 V. After completing the integration process **(g-i)**, the VM stabilizes at 1.817 V. Throughout the back-end of line process, the V_M shift remains within 6.2% of V_{dd}, which is well within the range of the tolerable noise margin.



c

SNM(V)	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)	(12)	(13)	(14)	(15)	(16)
(1)	0.981	0.924	0.624	0.408	0.299	0.604	0.442	0.491	0.724	0.714	0.584	0.539	0.321	0.724	0.181	0.373
(2)	0.858	0.895	0.768	0.482	0.251	0.608	0.568	0.479	0.798	0.628	0.482	0.491	0.299	0.668	0.328	0.212
(3)	0.833	0.884	0.432	0.534	0.301	0.683	0.634	0.261	0.668	0.803	0.583	0.634	0.481	0.635	0.583	0.523
(4)	0.554	0.681	0.586	0.518	0.286	0.796	0.558	0.281	0.748	0.758	0.518	0.432	0.303	0.558	0.518	0.432
(5)	0.621	0.539	0.474	0.372	0.256	0.407	0.357	0.225	0.625	0.678	0.427	0.392	0.238	0.567	0.327	0.364
(6)	0.601	0.784	0.649	0.506	0.345	0.768	0.646	0.293	0.626	0.763	0.506	0.537	0.474	0.724	0.506	0.678
(7)	0.723	0.525	0.704	0.473	0.129	0.717	0.677	0.362	0.624	0.679	0.473	0.692	0.226	0.646	0.437	0.579
(8)	0.704	0.652	0.542	0.381	0.199	0.364	0.421	0.419	0.603	0.371	0.484	0.339	0.257	0.315	0.381	0.561
(9)	0.612	0.423	0.661	0.612	0.528	0.501	0.641	0.578	0.755	0.612	0.521	0.498	0.434	0.671	0.421	0.427
(10)	0.629	0.532	0.492	0.492	0.187	0.729	0.702	0.337	0.776	0.719	0.469	0.571	0.483	0.603	0.462	0.429
(11)	0.703	0.548	0.472	0.507	0.468	0.782	0.742	0.292	0.792	0.637	0.507	0.424	0.283	0.542	0.507	0.512
(12)	0.428	0.587	0.686	0.628	0.328	0.684	0.686	0.271	0.633	0.681	0.628	0.508	0.227	0.688	0.328	0.553
(13)	0.512	0.492	0.561	0.612	0.187	0.681	0.681	0.378	0.554	0.631	0.342	0.498	0.348	0.361	0.222	0.214
(14)	0.629	0.432	0.429	0.629	0.272	0.742	0.729	0.337	0.775	0.592	0.462	0.571	0.158	0.478	0.463	0.287
(15)	0.387	0.385	0.472	0.507	0.459	0.528	0.641	0.292	0.537	0.547	0.507	0.228	0.182	0.471	0.507	0.336
(16)	0.468	0.351	0.326	0.456	0.194	0.659	0.354	0.215	0.584	0.638	0.473	0.186	0.172	0.238	0.323	0.429

Logic List

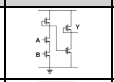
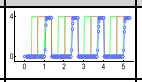
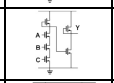
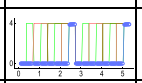
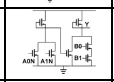
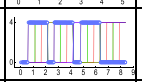
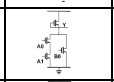
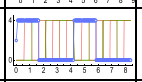
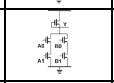
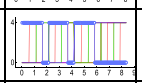
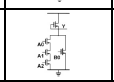
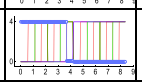
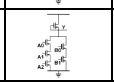
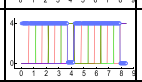
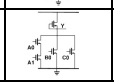
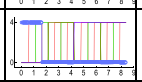
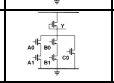
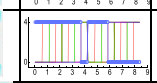
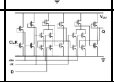
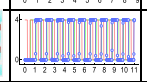
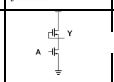
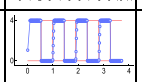
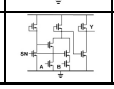
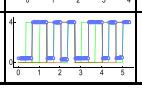
(1): AOI21
(2): AOI22
(3): AOI31
(4): AOI32
(5): AOI33
(6): AOI211
(7): AOI221
(8): AOI222
(9): OAI21
(10): OAI22
(11): OAI31
(12): OAI32
(13): OAI33
(14): OAI211
(15): OAI221
(16): OAI222

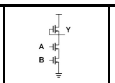
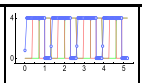
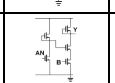
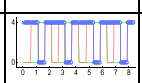
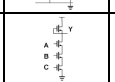
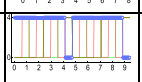
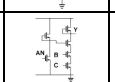
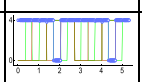
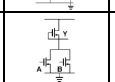
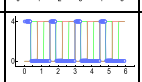
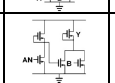
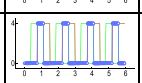
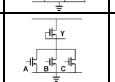
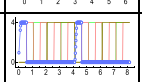
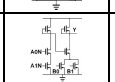
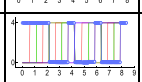
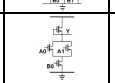
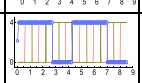
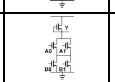
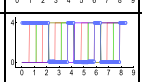
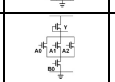
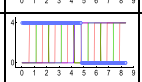
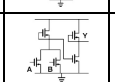
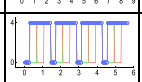
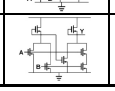
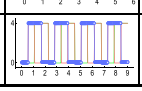
Extended Data Fig. 3 | Combined noise margin of 24 typical logic units. **(a-b)**, The noise margin was tested by adding an input inverter before the logic unit and an output inverter after the logic unit. **a** represents the results for NOR1 to NOR4 and **b** for NAND1 to NAND4. If the noise margin is less than 5% of V_{dd} (0.2 V), the logic unit is considered unsuitable for circuit composition. **c**, we summarized the full input-output margin maps for various single-stage logic gates and conducted an in-depth analysis of the specific impact of process variations on these margin maps. We have collated the minimum margin values for 16 combinations of single-stage logic gates operating at a voltage of 4 V. Among these, 11 logic gates have been selected as the practical PDK modeling units for application.

Logic	Description
AND2	2-input AND logic
AND3	3-input AND logic
AOI2BB2	2-2 AND-OR-Inverter logic, with 2 inverted input
AOI21	2-1 AND-OR-Inverter logic
AOI22	2-2 AND-OR-Inverter logic
AOI31	3-1 AND-OR-Inverter logic
AOI32	3-2 AND-OR-Inverter logic

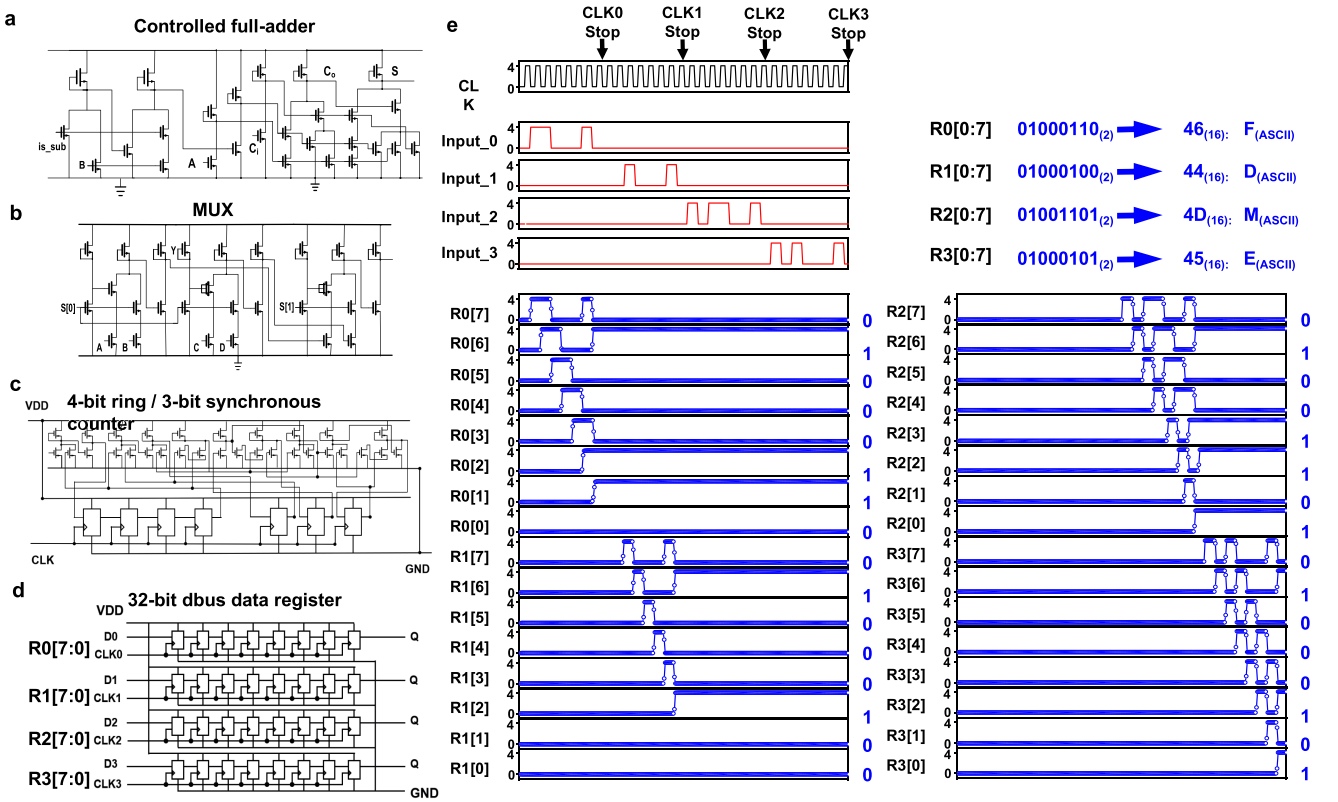
AOI211	2-1-1 AND-OR-Inverter logic
AOI221	2-2-1 AND-OR-Inverter logic
DFFHQ	positive edge-triggered D flip-flop
INV	inverter
MUX2	2-input multiplexer
NAND2	2-input NOT-AND logic
NAND2B	2-input NOT-AND logic, with 1 inverted input
NAND3	3-input NOT-AND logic
NAND3B	3-input NOT-AND logic, with 1 inverted input

NOR2	2-input NOT-OR logic
NOR2B	2-input NOT-OR logic, with 1 inverted input
NOR3	3-input NOT-OR logic
OAI2BB2	2-2 OR-AND-Inverter logic, with 2 inverted input
OAI21	2-1 OR-AND-Inverter logic
OAI22	2-2 OR-AND-Inverter logic
OAI31	3-1 OR-AND-Inverter logic
OR2	2-input OR logic
XOR2	2-input XOR logic

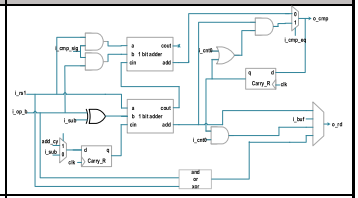
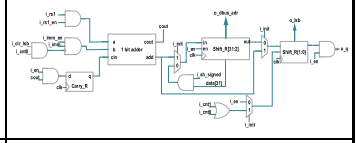
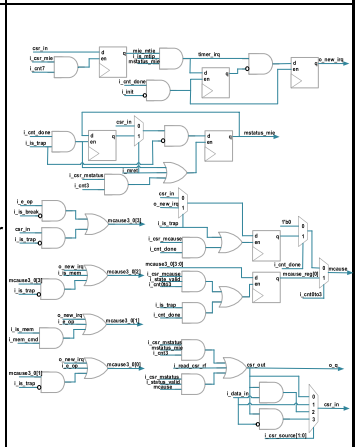
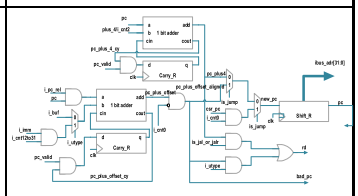
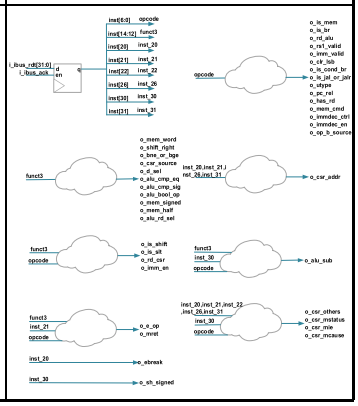
Logic	Schematic	Image & Layout	Experimental waveform	Logic function
AND2				$Y = A \cdot B$
AND3				$Y = A \cdot B \cdot C$
AOI2BB2				$Y = \overline{(A0N \cdot A1N)} + B0 \cdot B1$
AOI21				$Y = \overline{A0 \cdot A1 + B0}$
AOI22				$Y = \overline{A0 \cdot A1 + B0 \cdot B1}$
AOI31				$Y = \overline{A0 \cdot A1 \cdot A2 + B0}$
AOI32				$Y = \overline{A0 \cdot A1 \cdot A2 + B0 \cdot B1}$
AOI211				$Y = \overline{A0 \cdot A1 + B0 + C0}$
AOI221				$Y = \overline{A0 \cdot A1 + B0 \cdot B1 + C0}$
DFFHQ				$Q_{n+1} = D$ (@ positive clock edge)
INV				$Y = \overline{A}$
MUX2				$Y = \overline{SN} \cdot A + SN \cdot B$

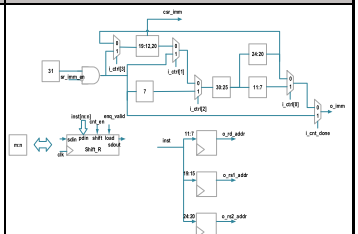
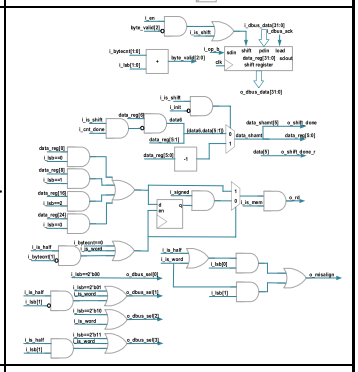
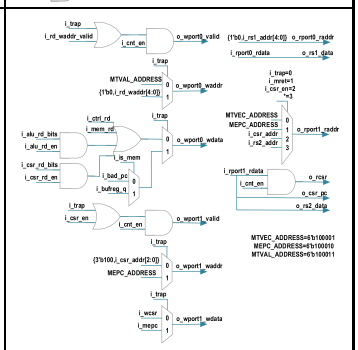
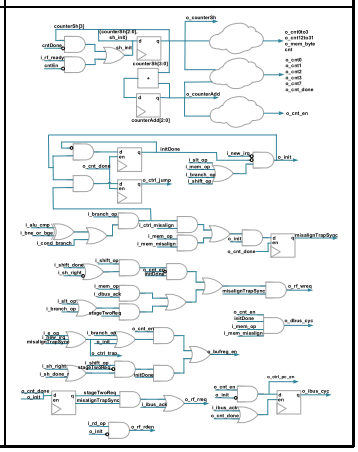
NAND2				$Y = \overline{A \cdot B}$
NAND2B				$Y = \overline{\overline{A} \cdot B}$
NAND3				$Y = \overline{A \cdot B \cdot C}$
NAND3B				$Y = \overline{\overline{A} \cdot B \cdot C}$
NOR2				$Y = \overline{A + B}$
NOR2B				$Y = \overline{\overline{A} + B}$
NOR3				$Y = \overline{A + B + C}$
OAI2BB2				$Y = \overline{(A0N + A1N) \cdot (B0 + B1)}$
OAI21				$Y = \overline{(A0 + A1) \cdot B0}$
OAI22				$Y = \overline{(A0 + A1) \cdot (B0 + B1)}$
OAI31				$Y = \overline{(A0 + A1 + A2) \cdot B0}$
OR2				$Y = A + B$
XOR2				$Y = A \oplus B$

Extended Data Fig. 4 | MoS_2 standard cell library. A complete table containing a total of 25 types of MoS_2 logic unit modules for our "2D_NMOS_lib" standard cell library, along with their corresponding brief description, microscopy image, the schematic of each cell, a typical measured waveform of each fabricated cell, and a truth table.

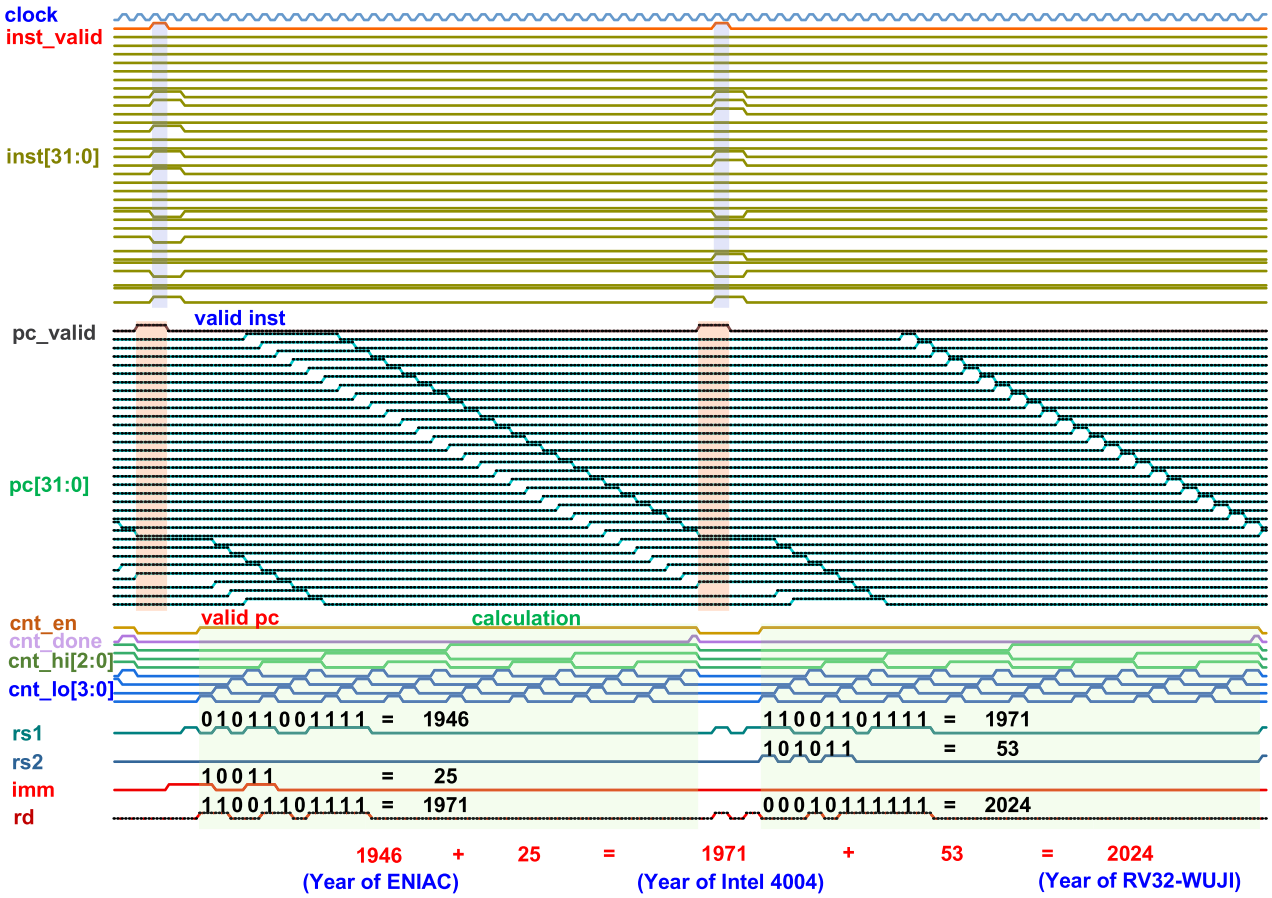


Extended Data Fig. 5 | The circuit schematics of four core functional modules in RX32-WUJI, and the typical measured waveforms from a core module of a 32-bit register. a, A 1-bit controlled adder module that includes an adder and a control logic, consisting of a total of 27 MoS_2 transistors. **b**, A selection module with four input signals and a total of 27 MoS_2 transistors, and its function is to select the appropriate signal output for the next stage by means of a coded selection. **c**, A 4-bit ring counter and a 3-bit synchronous counter, constructed using 156 MoS_2 transistors. It can perform both cyclic counting for a 4-bit signal and sequential counting up to 8. **d**, A 32-bit data register divided into four 8-bit register blocks, comprising a total of 576 MoS_2 transistors. This module can realize the storage and synchronous shift of data. **e**, The 32-bit register is divided into four 8-bit synchronous register blocks. Four sets of signals, 01000110, 01000100, 01001101, and 01000101, are input into the registers using a clock signal shifting input method. These signals correspond to the letters 'F', 'D', 'M', and 'E', respectively, according to the ASCII code.

Module	Function	Core units	Schematic
ALU	execute arithmetic and logic calculations	controlled full-adder	
Bufreg	buffer data calculate dbus address	32-bit shift-register	
Csr	control and status register	8-bit register	
Ctrl	store and update PC	32-bit PC register	
Decode	convert instructions into control signals	14-bit register	

Module	Function	Core units	Schematic
Immdec	extract immediate operand from instructions	27-bit register	
Mem_if	interface between CPU and memory	32-bit dbus data register	
Regfile_if	interface between CPU and Regfile	MUX	
State	control the execution of instructions by counters	4-bit ring counter and 3-bit synchronous counter	

Extended Data Fig. 6 | Main modules used in RV32-WUJI. This table lists the general function, core units, and schematic of each module separately. The majority of modules contain a multi-bit register as the core unit for data storage. The core units in ALU, Regfile_IF, and State are respectively the adder, multiplexer, and counter, used to implement data operations, i/o management, and count-based timing control.



Extended Data Fig. 7 | The result of digital computation by the 2D RV32 processor. In the first instruction, an operand stored in the register file, "1946" (the year ENIAC was manufactured), and another operand in the instruction as the immediate number, "25", are added together. On the first clock cycle of this instruction, the valid 32-bit PC is sent to the ibus with the *pc_valid* flag. The instruction is then sent to RV32-WUJI in the next clock cycle with the *inst_valid* flag. After several clock cycles for decoding, the counter starts counting while the computation begins: First, the lowest bits of "1946" ("0") and "25" ("1") are entered separately into the *ALU* as *rs1* and *imm*, whose names represent the data from the 1st source register and the immediate numbers. After the addition between the lowest bits is finished, the result bit is written back to the register file as *rd*, representing the destination register, and the carry is stored in the *ALU*. Then the second lowest bits are entered and added in the next clock cycle, while the carry stored in the *ALU* in the last clock cycle is included in the addition this time. The calculation continues until the counter reaches 32 and all 32-bit calculations are complete. A similar calculation is performed in the second instruction, except that both input operands, "1971" and "53", are from the register file. The final result is 2024, which is 1971 plus 53.

Extended Data Table 1 | Instruction set based on the 32-bit RISC-V integer instruction set architecture (RV32I base integer ISA)

inst	category	type	num. of stages	instruction																												
				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LUI	arithmetic	U	1	imm[31:12]																				rd					0110111				
AUIPC	arithmetic	U	1	imm[31:12]																				rd					0010111				
JAL	branch	J	2	imm[20][10:1][11][19:12]																				rd					1101111				
JALR	branch	I	2	imm[11:0]												rs1				0	0	0		rd					1100111				
BEQ	branch	B	2	imm[12][10:5]							rs2					rs1				0	0	0		imm[4:1][11]					1100011				
BNE	branch	B	2	imm[12][10:5]							rs2					rs1				0	0	1		imm[4:1][11]					1100011				
BLT	branch	B	2	imm[12][10:5]							rs2					rs1				1	0	0		imm[4:1][11]					1100011				
BGE	branch	B	2	imm[12][10:5]							rs2					rs1				1	0	1		imm[4:1][11]					1100011				
BLTU	branch	B	2	imm[12][10:5]							rs2					rs1				1	1	0		imm[4:1][11]					1100011				
BGEU	branch	B	2	imm[12][10:5]							rs2					rs1				1	1	1		imm[4:1][11]					1100011				
LB	memory	I	2	imm[11:0]												rs1				0	0	0		rd					0000011				
LH	memory	I	2	imm[11:0]												rs1				0	0	1		rd					0000011				
LW	memory	I	2	imm[11:0]												rs1				0	1	0		rd					0000011				
LBU	memory	I	2	imm[11:0]												rs1				1	0	0		rd					0000011				
LHU	memory	I	2	imm[11:0]												rs1				1	0	1		rd					0000011				
SB	memory	S	2	imm[11:5]							rs2					rs1				0	0	0		imm[4:0]					0100011				
SH	memory	S	2	imm[11:5]							rs2					rs1				0	0	1		imm[4:0]					0100011				
SW	memory	S	2	imm[11:5]							rs2					rs1				0	1	0		imm[4:0]					0100011				
ADDI	arithmetic	I	1	imm[11:0]												rs1				0	0	0		rd					0010011				
SLTI	arithmetic	I	2	imm[11:0]												rs1				0	1	0		rd					0010011				
SLTIU	arithmetic	I	2	imm[11:0]												rs1				0	1	1		rd					0010011				
XORI	arithmetic	I	1	imm[11:0]												rs1				1	0	0		rd					0010011				
ORI	arithmetic	I	1	imm[11:0]												rs1				1	1	0		rd					0010011				
ANDI	arithmetic	I	1	imm[11:0]												rs1				1	1	1		rd					0010011				
SLLI	shift	I	2	0000000							shamt					rs1				0	0	1		rd					0010011				
SRLI	shift	I	2	0000000							shamt					rs1				1	0	1		rd					0010011				
SRAI	shift	I	2	0100000							shamt					rs1				1	0	1		rd					0010011				
ADD	arithmetic	R	1	0000000							rs2					rs1				0	0	0		rd					0110011				
SUB	arithmetic	R	1	0100000							rs2					rs1				0	0	0		rd					0110011				
SLL	shift	R	2	0000000							rs2					rs1				0	0	1		rd					0110011				
SLT	arithmetic	R	2	0000000							rs2					rs1				0	1	0		rd					0110011				
SLTU	arithmetic	R	2	0000000							rs2					rs1				0	1	1		rd					0110011				
XOR	arithmetic	R	1	0000000							rs2					rs1				1	0	0		rd					0110011				
SRL	shift	R	2	0000000							rs2					rs1				1	0	1		rd					0110011				
SRA	shift	R	2	0100000							rs2					rs1				1	0	1		rd					0110011				
OR	arithmetic	R	1	0000000							rs2					rs1				1	1	0		rd					0110011				
AND	arithmetic	R	1	0000000							rs2					rs1				1	1	1		rd					0110011				

There are 37 instructions available for execution, including branch, memory access, and arithmetic and logic operations. Some instructions require one stage, or 32 clock cycles, to complete execution, while others require two stages. Branch and memory access instructions are typically two-stage, while most arithmetic and logic operation instructions are one-stage, except for shift instructions.

Extended Data Table 2 | "Datasheet" of RV32-WUJI

"Technology information and parameters"	"Values/Types"
Semiconductor material	MoS_2
Channel length L (μm)	3
Channel width W (μm)	10
Supply voltage (V)	4
Wafer diameter (inch)	4
Total Thickness (nm)	< 300
Number of material layers	9
Number of metal layers	4
Integrated Transistor #	5931
Operating frequency (Hz)	1 K
Power consumption (mW) ("1946+25=1971" and "1971+53=2024")	0.431 (@1kHz)
Maximum path delay (μs)	171
Maximum load capacitance (pF)	10
Maximum number of loaded logic gates	4
FET threshold voltage V_{TH} (V)	Avg: 1.8
FET sub-threshold swing (mV/dec)	100-160 (due to batch variations)
Load FET linear on-current (μA/μm)	Avg: 2.5
Drive FET linear on-current (μA/μm)	Avg: 1.2
FET current ON/OFF ratio	10^8~10^9 (due to batch variations)
FET hysteresis of transfer characteristic (mV)	Avg: 143

Extended Data Table 3 | Comparison functional demonstration of circuits based on 2D semiconductor

References	Material	Channel Length (μm)	Transistor integration scale	Function
25	MoS_2	2	115	Logic
26	MoS_2	15	156	Logic
39	MoS_2	0.4	100	In-Memory Computing
40	MoS_2	0.9	81	In-Memory Computing
41	MoS_2	1	32	Logic in Memory
42	MoS_2	5	400	Active-Matrix Displays
43	MoS_2	4.2	200	Active-Matrix Displays
44	MoS_2	5	186	Active Matrix of 2T1C
45	MoS_2/IGZO	7	24	2T0C
46	MoS_2	10	32	Logic
47	MoS_2	10	26	Logic
48	WSe_2	1	12	Logic
This Work	MoS_2	3	5931	Logic

The last row is our work, demonstrating the integration scale and functional presentation compared with other Works. The following references are cited in this table: refs. 25,26,39–48.